# COURSE PLAN

|  |  |
| --- | --- |
| Target | 50% (marks) |
| Level-1 | 40% (population) |
| Level-2 | 50% (population) |
| Level-3 | 60% (population) |

## Method of Evaluation

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| --- |
| **UG** |
| Internal assessment (50%)-Tests-Quizzes, Assignments/Project |
| Mid Examination (20%), Exam |
| End examination (30%), Exam |

|  |  |
| --- | --- |
| **Internal Assessment Component** | **Weightage in calculation of Internal Assessment (100 marks)** |
| Quiz 1 | 15% |
| Quiz 2 | 15% |
| Class Test 1 | 15% |
| Class Test 2 | 15% |
| Assignment 1/Project | 20% |
| Assignment 2/Project | 20% |

1. **Passing Criteria**

|  |  |
| --- | --- |
| **Scale** | **UG** |
| **Out of 10point scale** | SGPA – “5.0” in each semester CGPA – “5.0”  Min. Individual Course Grade – “C” Course Grade Point – “3.0” |

\*for UG, passing marks are 35/100 in a paper

1. **Prerequisite(s):** Basic Knowledge of computer systems, Concept of Digital Electronics
2. **Course Objectives**

To equip students with the necessary knowledge and skills to comprehend, analyze, and design digital computer systems, ensuring they can effectively develop and optimize software applications and systems.

## Pedagogy

* + Proper session plan
  + Presentation
  + Class Test
  + Quizzes
  + Assignments/Projects
  + Voice over Presentation & Video lectures
  + Performance Tests

1. **References**

|  |  |
| --- | --- |
| Text Books | 1. M. M. Mano, "Computer System Architecture", Revised 3rd Edition, Pearson Education, 2017. 2. Carl Hamacher, Zvonko Vranesic , Safwat Zaky, and Naraig Manjikian, "Computer Organization and Embedded Systems", 6th Edition, McGraw Hill, Standard Edition, 2023. 3. David A. Patterson, and John L. Hennessy, "Computer Organization and Design MIPS Edition: The Hardware/Software Interface", 5th Edition, The Morgan Kaufmann Series in Computer Architecture and Design, Morgan Kaufmann, 2020. |
| Web resources | NPTEL |
| Journals | Information about advanced research about any topics of syllabus from SCI/SCIE/Scopus |
| Reference books | 1. John P. Hayes, "Computer Architecture and Organization", 3rd Edition, McGraw-Hill Education, 2017. 2. William Stallings, "Computer Organization and Architecture: Designing for Performance", 11th Edition, Pearson, 2022. |

# GUIDELINES TO STUDY THE SUBJECT

## Instructions to Students:

1. Go through the 'Syllabus' uploaded on the My UPES- LMS platform to find out the Reading List.
2. Get your schedule and try to pace your studies as close to the timeline as possible.
3. Get your on-line lecture notes (Content, videos) at Lecture Notes section. These are our lecture notes. Make sure you use them during this course.
4. Check your LMS student portal regularly.
5. Go through study material.
6. Check mails and announcements on LMS student portal.
7. Keep updated with the posts, assignments and examinations which shall be conducted on the LMS student portal.
8. Be regular, so that you do not suffer in any way.
9. **Cell Phones and other Electronic Communication Devices:** Cell phones and other electronic communication devices are not permitted in classes during the Tests. Such devices MUST be turned off in the classroom.
10. **E-Mail and online learning tool:** Each student in the class should have an e-mail id and a pass word to access the LMS system regularly. Regularly, important information – Date of conducting class tests, guest lectures, via online learning tool. The best way to arrange meetings with us or ask specific questions is by email and prior appointment. All the assignments preferably should be uploaded on an online learning tool. Various research papers/reference material will be mailed/uploaded on online learning platform from time to time.
11. **Attendance:** Students are required to have a minimum attendance of 75% in each subject. Students with less than the said percentage shall NOT be allowed to appear in the end semester examination.

This much should be enough to get you organized and on your way to having a great semester! If you need us for anything, send your feedback through e-mail [to](mailto:abc@ddn.upes.ac.in) your concerned faculty. Please use an appropriate subject line to indicate your message details.

# RELATED OUTCOMES

1. **The expected outcomes of the Program:**

|  |  |
| --- | --- |
| PO1 | Engineering knowledge: Apply the knowledge of mathematics, science, engineering  fundamentals, and an engineering specialization to the solution of complex engineering problems. |
| PO2 | Problem analysis: Identify, formulate, review research literature, and analyze complex  engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences. |

|  |  |
| --- | --- |
| PO3 | Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental  considerations. |
| PO4 | Conduct investigations of complex problems: Use research-based knowledge and research  methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions. |
| PO5 | Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern  engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations. |
| PO6 | Engineer and society: Apply reasoning informed by contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice. |
| PO7 | Environment and sustainability: Understand the impact of professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development. |
| PO8 | Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of engineering practice. |
| PO9 | Individual and teamwork: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings. |
| PO10 | Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive  clear instructions. |
| PO11 | Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments. |
| PO12 | Life-long learning: Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change. |

1. **The expected outcomes of the Specific Program:**

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| --- | --- |
| PSO1 | Perform system and application programming using computer system concepts, the principles of data structures, algorithm development, problem-solving, and optimization techniques. |

|  |  |
| --- | --- |
| PSO2 | Apply software development and project management methodologies, integrating principles from both front-end and back-end development, and effectively utilize contemporary tools and technologies. |
| PSO3 | Exhibit a commitment to ethical practices, societal responsibilities, and continuous learning, contributing to the advancement of technology and addressing challenges in diverse computing domains. |

1. **The expected outcomes of the Specific Program:**

On completion of this course, the students will be able to

**CO1:** Analyze the components and organization of digital computers.

**CO2:** Apply knowledge of instruction codes, instruction formats, and addressing modes to analyze and design computer instructions in different CPU architectures.

**CO3:** Examine the design and organization of control units in digital computers to comprehend their role in executing instructions and managing system operations.

**CO4:** Analyze the organization and performance implications of memory units and input –output systems in digital computer systems.

**CO5:** Assess the benefits and challenges of pipelining computer architecture on system performance and throughput.

1. **Co-Relationship Matrix**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Program**  **Outcomes** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** | **PSO3** |
| **Course Outcomes** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **CO 1** | 1 |  | 2 | **-** | 1 | 1 | 1 | **-** | **-** | **-** | **-** | 3 | 2 | **-** | **-** |
| **CO 2** | 1 | 1 | 2 | **-** | 1 | 1 | 1 | **-** | **-** | **-** | **-** | 3 | 2 | **-** | **-** |
| **CO 3** | 1 | 1 | 2 | **-** | 1 | 1 | 1 | **-** | **-** | **-** | **-** | 3 | 2 | **-** | **-** |
| **CO 4** | 1 |  | 2 | **-** | 1 | 1 | 1 | **-** | **-** | **-** | **-** | 3 | 2 | **-** | **-** |
| **CO 5** | 1 | 1 | 2 | **-** | 1 | 1 | 1 | **-** | **-** | **-** | **-** | 3 | 2 | **-** | **-** |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Average** | 1 | 0.6 | 2 | **-** | 1 | 1 | 1 | **-** | **-** | **-** | **-** | 3 | 2 | **-** | **-** |

**1 – Weakly Mapped (Low) 2 – Moderately Mapped (Medium) 3 – Strongly Mapped (High) “\_” means there is no correlation**

1. **Course outcomes assessment plan:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **components**  **Course Outcomes** | **Quiz** | **Class Test** | **Lab Test** | **Project/Assignment** | **Any other** |
| **CO 1** | ☑ | ☑ | ☑ | ☑ | □ |
| **CO 2** | ☑ | ☑ | ☑ | ☑ | □ |
| **CO 3** | ☑ | ☑ | ☑ | ☑ | □ |
| **CO 4** | ☑ | ☑ | ☑ | ☑ | □ |
| **CO 5** | ☑ | ☑ | ☑ | ☑ | □ |

# OVERVIEW OF COURSE DELIVERY/BROAD PLAN OF COURSE COVERAGE

**Course Activities:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **S.**  **No.** | **Description** | **Planned** | | | **Actual** | | | **Remarks** |
| **From** | **To** | **No. of Ses** | **From** | **TO** | **No. of Ses** |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1.** | Digital Computers Unit I |  |  | 8 |  |  |  |  |
| **2.** | Basic Computer Organization and Design- Unit II |  |  | 7 |  |  |  |  |
| **3.** | Control Organization- Unit-III |  |  | 6 |  |  |  |  |
| **4.** | Memory Organization- Unit-IV |  |  | 8 |  |  |  |  |
| **5.** | Input Output Organization |  |  | 8 |  |  |  |  |
| **6.** | Pipelining |  |  | 8 |  |  |  |  |

# SESSION PLAN UNIT-I

**Digital Computers**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Session Plan | | | | Actual Delivery | | | |
| L |  |  | CO | L |  | To | CO |
| e | D |  | Ma | e | D | pic | Ac |
| ct | at |  | ppe | ct | at | s | hie |
| . | e | Topics to be Covered | d | . | e | Co | ved |

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| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  | ver ed |  |
| 1 |  | Introduction about digital computer, Why digital computer? Classification about computing and non-computing systems,  Overview of different blocks of computer | CO 1 |  |  |  |  |
| 2 |  | Introduction to CPU (Registers, ALU, Clock, Control unit), Memory, | CO 1 |  |  |  |  |
| 3 |  | I/O subsystems, Common Bus System (External and Internal Bus: Address Bus, Data Bus and Control Bus); | CO 1,C O2 |  |  |  |  |
| 4 |  | Evolution of Computer Systems, Von Neumann Architecture and Harvard Architecture | CO 1,C O2 |  |  |  |  |
| 5 |  | Big Endian and Little Endian, Signed Arithmetic- Addition, Subtraction, Multiplication, | CO 1,C O2 |  |  |  |  |
| 6 |  | Data representation: Number System, r complement and r-1  complement arithmetic, Unsigned and Signed number representation, Preliminary idea of combinational circuits | CO 1,C O2 |  |  |  |  |
| 7 |  | Register Transfer Language (RTL) and Micro operations (Arithmetic, Logical and Shift micro operations), | CO 1,C O2 |  |  |  |  |
| 8 |  | Arithmetic Logic and Shift unit hardware implementation,Register transfer, Bus and memory transfer | CO 1,C O2 |  |  |  |  |

# UNIT-II

**Basic Computer Organization and Design**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Session Plan | | | | Actual Delivery | | | |
| Lec t. | Dat e | Topics to be Covered | CO  Mapp ed | Lec t. | Dat e | Topic s Cover  ed | CO  Achiev ed |
| 1 |  | Instruction codes and format | CO2 |  |  |  |  |
| 2 |  | Stored program organization | CO2 |  |  |  |  |
| 3 |  | Instruction cycles, Instruction Formats, Instruction types | CO2 |  |  |  |  |
| 4 |  | Timing and control, Instruction and Instruction sequencing | CO2 |  |  |  |  |
| 5 |  | Addressing types, Memory Reference | CO2 |  |  |  |  |
| 6 |  | Stack organization | CO2 |  |  |  |  |
| 7 |  | Some common CPU architectures(Intel IA-32 Architecture, ARM) | CO2 |  |  |  |  |

# UNIT-III

**Control Unit Organization**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Session Plan | | | | Actual Delivery | | | |
| Lect  . | Date | Topics to be Covered | CO  Mapped | Lect  . | Date | Topics Covere d | CO  Ac hie  ve d |
| 1 |  | Introduction Control Unit Design, Hardwired Control Unit and Timing Signals | CO3 |  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 2 |  | Microprogrammed control unit:  control memory, Address sequencing | CO3 |  |  |  |  |
| 3 |  | Designing of microprogrammed control uni Control Transfer, Fetch Cycle | CO3 |  |  |  |  |
| 4 |  | Comparison of hardwired and microprogrammed control units,  RISC and CISC Processors | CO3 |  |  |  |  |
| 5 |  | Arithmetic and logic unit design | CO3,C O1 |  |  |  |  |
| 6 |  | Designing a hypothetical processor with minimum number of Instruction | CO3,C O2 |  |  |  |  |

# UNIT-IV

**Memory Organization**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Session Plan | | | | Actual Delivery | | | |
| Le ct. | D  at e | Topics to be Covered | CO  Map ped | Le ct. | D  at e | Topi cs Cov  ered | CO  Achi eved |
| 1 |  | Memory Hierarchy ,memory Locations & Addresses,  Semiconductor Memory, Static and Dynamic Memory | CO1,  CO4 |  |  |  |  |
| 2 |  | Main Memory, Memory address map, | CO1, CO4 |  |  |  |  |
| 3 |  | Auxiliary Memory, Associative Memory, hardware organization Cache Memory | CO1, CO4 |  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 4 |  | Secondary Memories: Optical Magnetic Tape, Magnetic Disk and Controllers. | CO1, CO4 |  |  |  |  |
| 5 |  | Cache Memory: Principle of Locality, Cache mapping techniques | CO4 |  |  |  |  |
| 6 |  | Virtual memory, address space and memory space | CO4 |  |  |  |  |
| 7 |  | Memory management hardware, segmented page mapping | CO4 |  |  |  |  |
| 8 |  | Memory protection and numerical example | CO4 |  |  |  |  |

# UNIT-V

**Input Output Organization**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Session Plan | | | | Actual Delivery | | | |
| Lect. | Date | Topics to be Covered | CO  Mapped | Lect. | Date | Topics Covered | CO  Achieved |
| 1 |  | I/O and their brief description | CO4 |  |  |  |  |
| 2 |  | Bus Interface, Bus arbitration, Data Transfer | CO4,CO1 |  |  |  |  |
| 3 |  | Asynchronous data transfer and modes of transfer | CO4 |  |  |  |  |
| 4 |  | Types of Interrupts, I/O Interrupts,  priority interrupt | CO4 |  |  |  |  |
| 5 |  | Interrupt cycle, software routines | CO4 |  |  |  |  |
| 6 |  | Direct Memory Access, controller and transfer | CO4 |  |  |  |  |
| 7 |  | Input output processor | CO4 |  |  |  |  |
| 8 |  | Serial communication and its protocols | CO4 |  |  |  |  |

# UNIT-VI

**Pipelining**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Session Plan | | | | Actual Delivery | | | |
|  | | | |  | | | |
| Le ct. | Date | Topics to be Covered | CO  Mappe d | Lect  . | Date | Topics Covered | CO  Achieve d |
| 1 |  | Pipelining general consideration | CO5 |  |  |  |  |
| 2 |  | Arithmetic pipeline, Instruction pipeline | CO5 |  |  |  |  |
| 3 |  | Shared memory and distributed memory | CO5 |  |  |  |  |
| 4 |  | Vector processing | CO5 |  |  |  |  |
| 5 |  | Array processors | CO5 |  |  |  |  |
| 6 |  | Four-Segment Instruction Pipeline Pipelining Conflicts: Resource conflicts | CO5 |  |  |  |  |
| 7 |  | RISC and CISC pipeline | CO5 |  |  |  |  |
| 8 |  | Pipelining in ColdFire Processors, Pipelining in Intel Processors | CO5 |  |  |  |  |

# PERIODIC MONITORING

**Actual date of completion and remarks, if any**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Components** | **From** | **To** | **From** | **To** | **From** | **To** |
| **Duration (Mention from and to dates)** |  |  |  |  |  |  |
| **Percentage of Syllabus covered** |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Lectures** | **Planned** |  |  |  |  |  |  |
| **Taken** |  |  |  |  |  |  |
| **Tutorials/Discussions** | **Planned** |  |  |  |  |  |  |
| **Taken** |  |  |  |  |  |  |
| **Test/quizzes** | **Planned** |  |  |  |  |  |  |
| **Taken** |  |  |  |  |  |  |
| **CO's Addressed** |  |  |  |  |  |  |
| **CO's Achieved** |  |  |  |  |  |  |
| **Assignments** | **Planned** |  |  |  |  |  |  |
| **Taken** |  |  |  |  |  |  |
| **CO's Addressed** |  |  |  |  |  |  |
| **CO's Achieved** |  |  |  |  |  |  |
| **Signature of Faculty** | |  | |  | |  | |
| **Head of the Department** | |  | |  | |  | |
| **A.M.R.C** | |  | |  | |  | |

# PERIODIC MONITORING

**Attainment of the Course (Learning) Outcomes:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Components** | **Attainment level** | **Action plan** | **Remark**  **(AMC)** |
| **Assignment** | **CO1:** |  |  |
| **CO2:** |  |  |
| **CO3:** |  |  |
| **CO4:** |  |  |
| **Quiz/test** | **CO1:** |  |  |
| **CO2:** |  |  |
| **CO3:** |  |  |
| **CO4:** |  |  |
| **Mid Semester** | **CO1:** |  |  |
| **CO2:** |  |  |
| **CO3:** |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
|  | **CO4:** |  |  |
| **End Semester** | **CO1:** |  |  |
| **CO2:** |  |  |
| **CO3:** |  |  |
| **CO4:** |  |  |
| **Any Other** | **CO1:** |  |  |
| **CO2:** |  |  |
| **CO3:** |  |  |
| **CO4:** |  |  |

**Signature of HOD/ Dean Signature of Faculty**

**Date Date**

# INDIRECT ASSESSMENT

## Sample format for Indirect Assessment of Course outcomes:

|  |
| --- |
| NAME: |
| ENROLLMENT NO: |
| SAP ID: |
| COURSE: |
| PROGRAM: |

Please rate the following aspects of course outcomes of --.

Use the scale 1-3\*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| course Outcomes | Statement | 1 | 2 | 3 |
| CO1 |  |  |  |  |
| CO2 |  |  |  |  |
| CO3 |  |  |  |  |
| CO4 |  |  |  |  |
| CO5 |  |  |  |  |
| CO6 |  |  |  |  |

# INSTRUCTIONS FOR FACULTY

## Instructions for faculty

* Faculty should keep track of the students with low attendance and counsel them regularly.
* Course coordinator will arrange to communicate the short attendance (as per UPES policy) cases to the students and their parents monthly.
* Topics covered in each class should be recorded in the table of RECORD OF CLASS TEACHING (Suggested Format).
* Internal assessment marks should be communicated to the students twice in a semester.
* The file will be audited by respective Academic Monitoring and Review Committee (AMRC) members for theory as well as for lab as per AMRC schedule.
* The faculty is required to maintain these files for a period of at least three years.
* This register should be handed over to the head of department, whenever the faculty member goes on long leave or leaves the Colleges/University.
* For labs, continuous evaluation format (break-up given in the guidelines for result preparation in the same file) should be followed.
* Department should monitor the actual execution of the components of continuous lab evaluation regularly.
* Instructor should maintain record of experiments conducted by the students in the lab weekly.
* Instructor should promote students for self-study and to make concept diary, due weightage in the internal should be given under faculty assessment for the same.
* Course outcome assessment: To assess the fulfilment of course outcomes two different approaches have been decided. Degree of fulfillment of course outcomes will be assessed in different ways through direct assessment and indirect assessment. In Direct Assessment, it is measured through quizzes, tests, assignment, Mid-term and/or End-term examinations. It is suggested that each examination is designed in such a way that it can address one or two outcomes (depending upon the course completion). Indirect assessment is done through the student survey which needs to be designed by the faculty (sample format is given below) and it shall be conducted towards the end of course completion. The evaluation of the achievement of the Course Outcomes shall be done by analyzing the inputs received through Direct and Indirect Assessments and then corrective actions suggested for further improvement.

# CHECKLIST

**Check list Course Outcomes Attainment (COA)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **SI.N**  **o** | **Description** | **Date of Submissio**  **n** | **Checke d** | **Remarks** |
| 1 | Class Tests marks |  |  |  |
| 2 | Quiz marks |  |  |  |
| 3 | Assignment marks |  |  |  |
| 4 | Mid Semester Marks |  |  |  |
| 5 | End Semester Marks |  |  |  |
| 6 | Check in COA format |  |  |  |
| 7 | Whether respective CO of Class tests,  Quiz’s, Assignments, Mid and End semester maximum marks entered or not |  |  |  |
| 8 | Ensure that all data got filled as per requirement |  |  |  |
| 9 | Copy of quiz paper with the model answer and two/three answer sheets |  |  |  |
| 10 | Copies of all test papers with two/three answer sheets |  |  |  |
| 11 | Copies of all assignments with two or three model assignments |  |  |  |
| 12 | Manual attendance sheet |  |  |  |
| 13 | Copy of faculty time table |  |  |  |
| 14 | Course Plan |  |  |  |
| 15 | Class Tests, Quiz and assignment marks as per COs |  |  |  |
| 16 | Copy of midterm examination paper and model  solution |  |  |  |
| 17 | Copy of end term examination paper and model solution |  |  |  |
| 18 | List of minor/major project work given to the student |  |  |  |
| 19 | Detailed internal assessment sheet |  |  |  |
| 20 | Copy of final grade sheet (which was submitted to SRE) must be attached at the end of semester |  |  |  |
| 21 | Copy of quiz /test conducted for lab |  |  |  |
| 22 | Rubrics wise marks in Lab ( Day to day evaluation sheet) |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 23 | Copy of course attainment sheet (both pages) |  |  |  |
| 24 | Indirect Attainment Sheet |  |  |  |

**Signature of HOD/ Dean Signature of Faculty**

**Date Date**

**Planning for Remedial Classes**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Sl.**  **No.** | **Name of Student** | **Roll No.** | **Sap ID** | **Mid Sem Marks** | **Remedial Classes Held** | | | | | | | **Class test on the basis of**  **Remedial Classes** | **End Sem Marks** | **Improvement (Y/N)** |
| **Date** |  |  |  |  |  |  |
| **Venue** |  |  |  |  |  |  |
| **Time** |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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**Signature of HOD/ Dean Signature of Faculty**

**Date Date**